DETECTOR CONTROLLERS FOR GALILEO TELESCOPE, A PROGRESS REPORT

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Abstract

The Telescopio Nazionale Galileo (TNG) will support a large set of visual and near IR detectors at the focal plane. An important requirement for this crucial part of the telescope is to provide a set of specific detector controllers with shared hardware and software, in order to optimize and simplify the operations during maintenance and observation. A report on the current status of the project is here presented.

1. Introduction

The GALILEO telescope will require an extended set of CCD based cameras for the normal operation of focal plane instrumentation, moreover CCD cameras will be also required for the autoguiding and the active-optics system (Shack-Hartman analyzer). Some other CCD systems will be needed, in short time, for the activity of qualification of the optics system and for seeing-monitoring purposes. The aim of this paper is to present the current status of the CCD controller architecture for the Galileo cameras that meets the requirements briefly described in the next section.

2. CCD Camera Controller Requirements

We have considered as possible detector for the GALILEO telescope focal planes CCDs with more than 1K x 1K elements and multi-quadrant readout. The case of a 2 x 2 mosaic has also been taken into account. The CCD CONTROLLER is divided in two interacting parts: the CCD ANALOG ELECTRONICS and the CCD SEQUENCER. These two subsystems are directly interfaced with the detector cryostat and the control-computer respectively.

The functions supported by the CCD ANALOG ELECTRONICS are: a)CCD output signal processing and digitalization, b) CCD bias voltages generation, clocks level translation, and buffering, c)handling of mosaic focal-plane, d) cryostat temperature monitoring and controlling.

This section will support the readout of CCDs with more than two independent channels reducing the readout time. Analog processor inputs should be differential in order to minimize the EMI interference. All steady voltage levels should be monitored. A telemetry cycle should be repeated at a programmable rate. BIAS sources should be programmable. It is important to have different selectable readout speeds, optimized for performance and set-up purposes (some CCDs require long pixel time for best performance). If speed switching is available also switching between sets of pedestal, gain and time-constant parameters will be provided.

The functions supported by the CCD SEQUENCER are: a) clock waveform generation for CCD and signal processor, b)set and monitoring of CCD bias levels (clocks and analog levels), c) handling of local data-buffer and telemetry file making up, d) commands reception and handling, e) shutter handling.

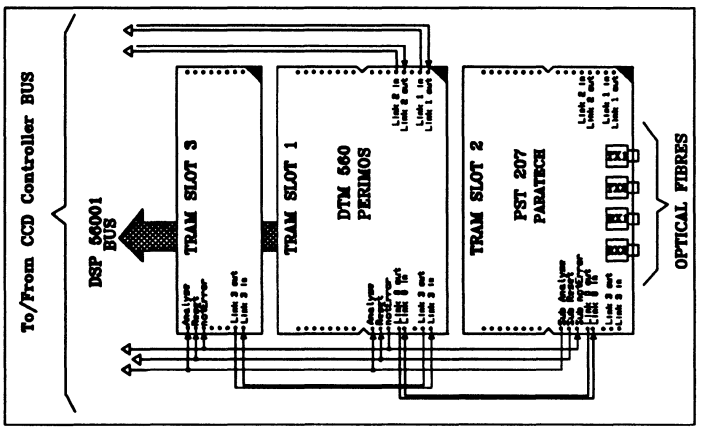

Figure 1: CCD Sequencer Motherboard block diagram

CCD readout modes must be possible as: a) full frame, b) only a set of predefined boxes with fast skip of unwanted pixels, c) with binning, d) in drift scan mode.

When in drift scan mode, synchronization should be externally provided.

The use of 2 × 2 CCD mosaic will be supported, and each CCD must be readable on 2 (or 4) outputs. In this case the readout time must be compatible with a single chip system. The output image must be "on fly" reformatted in order to simulate a single sensor having the full mosaic size. The chip intergaps must be filled by overscanned pixels.

3. CCD Sequencer

The heart of the CCD programmable sequencer is a standard TRAM module (DTM560) mounting a couple of high speed processors: a 16 bit **T222 INMOS transputer** and a 24 bit 56001 MOTOROLA DSP. The selected architecture for the sequencer meets the requirements described above. Transputer and DSP can communicate data and application SW through a set of shared memory locations. Thanks to the simple reconfigurable networking scheme embedded on the transputer, fast communication of data and commands is easily implementable with little extra hardware.

The CCDC sequencer (CCDSQ) is mounted on a single eurocard board (160 × 100 mm). This board acts also as motherboard for three standard TRAM service slots. The distribution of TRAM slots is reported in Figure 1. Part of the electronics dedicated to the generation of programmable sequences from the DSP is directly mounted on the motherboard.

Communication from the DSP bus and the motherboard is obtained through a couple of sockets (one on the TRAM side and the complementary on the motherboard side), so the DSP TRAM module must be plugged always on the same set of slots (TRAM slot 1 is reserved to the DSP module). The DTM560 TRAM module is a customized version carring the DSP bus outside the board. The main functional parts of the CCDSQ are shown in Figure 2.

Communication with the external world is obtained through the transputer *link 0* which is carried to the TRAM slot 1 and converted to an optical-fibre link. The TRAM slot 2 is always filled by the PST207 TRAM module holding a four fibre-optic communication system. TRAM slot 3 is free to be linked to other TRAM expansions; this option is allowed by the *link 3* from DTM560 which is carried to slot 3 allowing expansion support. *Link 1* and *link 2* from DTM560 are carried to the controller BUS, hence external TRAM modules can be mounted on expansion cards.

All communication functions are supported by the DTM560 T222 transputer through links (with the exception of DSP communication which is memory mapped) while generation of sequences are supported by the DSP. In particular the TRANSPUTER performs the boot of executable (TRANSPUTER and DSP), the handling of fibre-optic communication (commands, telemetry and data), data exchange and

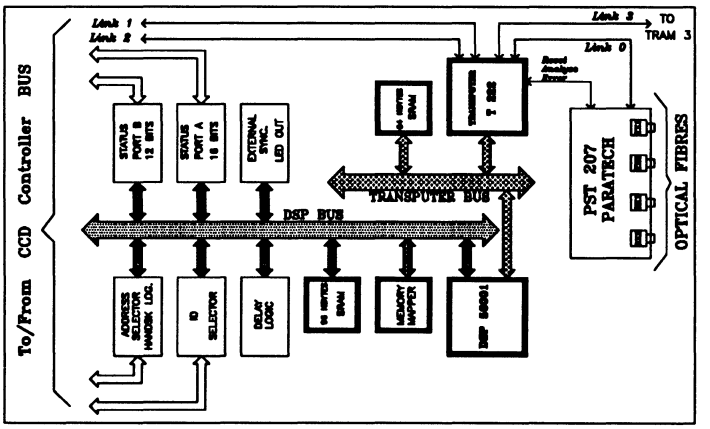

Figure 2: Functions of the CCD Sequencer board

dispatch of commands to DSP, the data collection and transmission to the root system and also the communication with expansion TRAMs.

While the DSP performs the generation of sequences, the data collection and the execution of commands from the T222.

Sequences can be generated in two ports: PORT A that allows 16 independent sequencer status lines and PORT B that allows 12 independent sequencer status lines. The generation of sequences is based on the output of a status word from a given table to a port at a given address followed by a delay loop. In order to handle delays with high time resolution (about 100 ns) it is mandatory to generate the delay with hardwired electronics instead of COMPARE/BRANCH software loops. An 8-bit counter is programmed with the upper 8 bits of the DSP 24 bits word, the lower 16 bits are used as programmable sequencer lines. The counter holds the DSP in WAIT state until the counter rollover; each tick corresponds to 100 ns (DSP at 20 MHz), so a maximum delay of 25.6 μs can be programmed. Should bigger delays needed, they can be obtained by conventional SW loops or by repeating the status output until the first change on the output is required.

The DSP circuit is completed with a card ID selector (7 readable dip switches), an external opto-coupled sync port, a programmable front panel LED, a switch to select the use of the X or Y DSP bus for CCD functions and an address decoder to handle internal and external memory mapped functions. The card ID selector is intended to be used by the TRANSPUTER for handling of link rooting of messages when various CCDSQ are connected to the network.

The external sync. port can be used to force CCD readouts (full frame or one line at time) following external stimuli (I.E. drift scan operation).

The fibre-optic link is handled by a two-size TRAM module (PST207) made by PARATECH England. This module (see ref.3) can be configured in order to handle communication across four optical fibres to carry one selectable transputer link (link 0 or 1 or 2 or 3) and the NOT-ERROR, the ANALYZE and the RESET signals.

One PST207 module is mounted on the CCDSQ board while the companion module will be mounted on the host-computer (PC or VME crate). In order to obtain the correct handling of signals the PST207 module mounted on the CCDSQ will send and receive the control singals through the ancillary pins called: SUBSYSTEM RESET, SUBSYSTEM ANALIZE and SUBSYSTEM NOT-ERROR.

4. Programmable Bias Generator

The board that generates the Bias levels has the following features:

- 32 buffered output voltages providing at least 10 mA. These are programmable through 8-bit D/A converters with serial loading (DAC 8800 PMI)

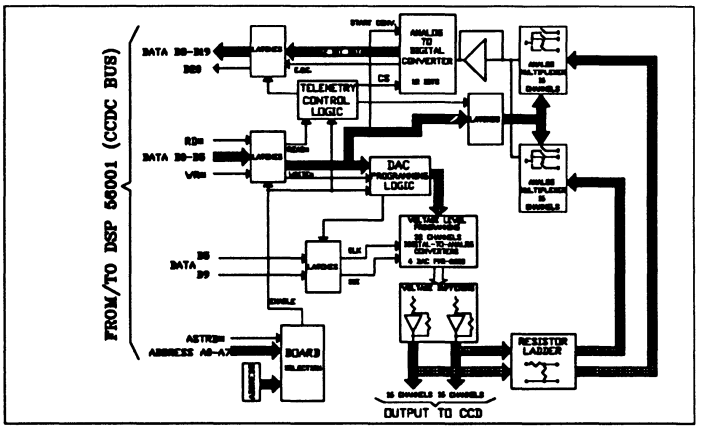

Figure 3: Programmable Bias block diagram

- level converter using a resistor ladder at each operational amplifier output for telemetry
- two 16/1 multiplexers with selection latch allowing the choice between 32 analog signals
- 12-bit ADC with 15 μs conversion time used for telemetry
- DSP data-bus used for ADC programming and telemetry
- board addressing and control logic for D/A programming and multiplexers driving.

The board is a single euro and is realized by using the *"Surface Mount Devices"* technology. Furthermore the board provides internally accurate reference voltages generator for DAC, ADC, and OPAMP (+5 V, +10 V, -10 V). The +15 V, - 15 V (V+ and V-) utilized for the remaining electronics are generated by using a temperature compensed voltage reference LM 399 and some operational amplifiers.

The design of the part concerning the bias is based on the PMI 8800 (Precesion Monolitics) which consists of octal 8-bit digital-to-analog converters (DAC), provided by serial addressing and data setting. The part concerning the voltage levels monitoring is based on the ADC 674A (Burr Brown). Figure 3 shows the block diagram of the whole board. The logical scheme can be divided in four sections: a) the board selection, b) the logic control, c) the voltage level programming, d) the signal levels multiplexing and telemetry.

Each digital-to-analog converter contained on a PMI 8800 is programmed through three lines: the Serial Data Input (SDI), the clock (CLK) and the Load (LD). The DAC output is unable to drive directly other devices, so we utilise operational amplifiers to buffer the output. The chip used to buffer the DAC output voltages is the OP 490 which contains four operational amplifiers capable of providing 20 mA output current. Telemetry is performed through a ADC 674A manufactured by Burr- Brown (12 bits, conv. time = 15 μs) and two Mux 16 by PMI. The logic of selection maintains the status of the addressing and selection lines of multiplexers till the next addressing.

By using the bipolar input -10 +10 of the ADC, the voltages coming from buffers are converted into the appropriate range. This is achieved by using resistor ladder at the input of the multiplexers.

REFERENCES

1. PERIMOS - DTM560 DSP-TRAM User Manual
2. PERIMOS - DTM560 TOOLBOX User Manual
3. PARATECH - PST207 Fibre-Optic TRAM manual
4. INMOS - D7205A TOOLSET development SW